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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/978,183	10/17/2001	Satoshi Oshima	62807-016	3969

7590 10/21/2004

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EXAMINER	
MCCARTHY, CHRISTOPHER S	
ART UNIT	**PAPER NUMBER**
2113	

DATE MAILED: 10/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/978,183	OSHIMA ET AL.	
	Examiner	Art Unit	
	Christopher S. McCarthy	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 August 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4,5 and 8-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4,5 and 8-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *Response to arguments*.

DETAILED ACTION

1. Claims 1, 4-5, 8-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Poisner U.S. Patent 6,012,154, as cited in prior office action, which was mailed on 5/5/2004.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 4-5, 8-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Poisner U.S. Patent 6,012,154.

As per claim 1, Poisner teaches a method of supervising a failure of a system using a plurality of timers, comprising the steps of: (a) activating one of said plurality of timers (column 6, lines 29-48; column 1, lines 50-54) and determining whether said one timer is reset or not (column 2, lines 31-34); (b) counting down said activated timer if not reset (column 2, lines 31-34, 57-60); (c) determining whether said activated timer has gone time out at a predetermined time (column 2, lines 36-39); (d) generating a signal for recovery from the failure in the case where said activated timer has gone time out (column 2, lines 36-53), and when said signal for recovery is generated, executing a corresponding one of the steps of (i) setting a flag, (ii) outputting an interrupt signal, (iii) outputting a non-maskable interrupt and (iv) outputting a

system reset signal; and (e) repeating (a) to (d) for another of said plurality of timers if the failure cannot be recovered after step (d) (column 4, lines 1-13, 60-65; column 2, lines 31-53), wherein each time said signal for recovery is generated, a corresponding one of steps (i) to (iv) is executed in a manner that steps (i) to (iv) are executed sequentially one by one when steps (a) to (e) are repeatedly executed, thereby recovering from the failure in accordance with the degree of the failure progressively each time said step (e) is executed (column 4, lines 1-13, 60-65; column 2, lines 31-53), and wherein: a plurality of registers are provided (column 4, lines 60-65), a plurality of conditions are respectively set for resetting said plurality of timers, said plurality of conditions corresponds to a plural sets of values set in a plurality of registers, respectively, and a reset to be performed on one of said plurality of registers corresponds to one of said plurality of conditions each time said step (e) is executed (column 4, lines 1-13, 60-65).

As per claim 4, Poisner teaches a failure supervising method according to claim 1, wherein the step executed in accordance with said signal generated in said step (d) is recorded (column 4, line 66 – column 5, line 28), wherein a record is inherently kept of the last interrupt so the process knows which interrupt to activate next.

As per claim 5, Poisner teaches an apparatus for supervising a failure of a system using a plurality of timers and a plurality of registers (column 6, lines 29-48; column 1, lines 50-54), comprising: (a) means for activating one of said plurality of timers timer and determining whether said activated timer is reset or not (column 2, lines 31-34); (b) means for counting down said activated timer if not reset (column 2, lines 31-34, 57-60); (c) means for determining whether said activated timer has gone time out at a predetermined time (column 2, lines 36-39); (d) means for generating a signal for recovery from the failure in the case where said activated

timer has gone time out (column 2, lines 36-53); and (e) means for executing a corresponding one of the steps of (i) setting a flag, (ii) outputting an interrupt signal, (iii) outputting a non-maskable interrupt and (iv) outputting a system reset signal , responsive to said signal being generated; (f) means for activating said means (a) to (e) for another one of said plurality of timers if the failure cannot be recovered after activating said means (e) (column 4, lines 1-13, 60-65; column 2, lines 31-53), wherein each time said signal for recovery is generated, a corresponding one of steps (i) to (iv) is executed in a manner that steps (i) to (iv) are executed sequentially one by one when steps (a) to (e) are repeatedly executed, thereby recovering from the failure in accordance with the degree of the failure progressively each time said means (f) is executed (column 4, lines 1-13, 60-65; column 2, lines 31-53), wherein; a plurality of conditions are respectively set for resetting said plurality of timers, said plurality of conditions corresponds to a plural sets of values set in a plurality of registers, respectively, and a reset to be performed on one of said plurality of registers corresponds to one of said plurality of conditions each time said means (f) is executed (column 4, lines 1-13, 60-65).

As per claim 8, Poisner teaches a failure supervising apparatus according to claim 5, wherein said signal generating means includes means for recording the step executed in accordance with said generated signal (column 4, line 66 – column 5, line 28), wherein a record is inherently kept of the last interrupt so the process knows which interrupt to activate next.

As per claim 9, Poisner teaches a method of supervising a failure of a system using a plurality of timers (column 6, lines 29-48; column 1, lines 50-54), comprising the steps of: (a) counting down said one of plurality of timers in the case where the said one timer is activated and is not reset (column 2, lines 31-34, 57-60); (b) generating a signal for recovering from the

failure in the case where said timer goes out at a predetermined time (column 2, lines 36-39), and when said signal for recovery is generated, executing a corresponding one of the steps of (i) setting a flag, (ii) outputting an interrupt signal, (iii) outputting a non-maskable interrupt and (iv) outputting a system reset signal; and (c) in the case where said system fails to recover from the failure, repeatedly executing the steps (a) and (b) for another one of said plurality of timers (column 4,, lines 1-13; column 4, lines 1-13, 60-65; column 2, lines 31-53), wherein each time said signal for recovery is generated, a corresponding one of steps (i) to (iv) is executed in a manner that steps (i) to (iv) are executed sequentially one by one when steps (a) to (c) are repeatedly executed, thereby recovering from the failure in accordance with the degree of the failure progressively each time said step (c) is executed (column 4, lines 1-13, 60-65; column 2, lines 31-53), and wherein: a plurality of registers are provided (column 4, lines 60-65), a plurality of conditions are respectively set for resetting said plurality of timers, said plurality of conditions corresponds to a plural sets of values set in a plurality of registers, respectively, and a reset to be performed on one of said plurality of registers corresponds to one of said plurality of conditions each time said step (c) is executed (column 4, lines 1-13, 60-65).

As per claim 10, Poisner teaches a method of claim 1, wherein information is written into said plurality of registers as said values from a supervisee (column 4, line 66 – column 5, line 9, wherein, the software agent is the active supervisee.

As per claim 11, Poisner teaches the apparatus of claim 5, wherein information is written into said plurality of registers as said values from a supervisee (column 4, line 66 – column 5, line 9, wherein, the software agent is the active supervisee.

As per claim 12, Poisner teaches the method of claim 9, wherein information is written into said plurality of registers as said values from a supervisee (column 4, line 66 – column 5, line 9, wherein, the software agent is the active supervisee.

Response to Arguments

3. Applicant's arguments filed 8/5/2004 have been fully considered but they are not persuasive.

The applicant has argued that Poisner does not teach the utilization of a plurality of timers and a plurality of registers. The examiner respectfully disagrees. Poisner suggests, in claim 9, the use of a first timer and a second timer. Teaching a second timer fulfills the term of a "plurality" of timers as having more than one. In the description of Poisner, he teaches the use of register for use in a timer (column 4, line 66 – column 5, line 9). Since Poisner does suggest the use of a plurality of timers in claim 9, then it is deduced that each timer embodies the same elements. Each timer has a register and there are multiple timers, therefore, there are multiple registers. Furthermore, the examiner requests that the applicant point out in the present invention where the timers are physically distinct as argued. In light of the above argument, all rejected claims stand.

Conclusion

4. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher S. McCarthy whose telephone number is (571)272-3651. The examiner can normally be reached on M-F, 9 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571)272-3645. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

csm

October 18, 2004

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